Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/051,335	TAKAYAMA ET AL.
	Examiner	Art Unit
	Satish S. Rampuria	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *19 October 2001, preliminary amendment*.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *29-32 and 45-48* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *29-32 and 45-48* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☒ Certified copies of the priority documents have been received in Application No. *09/301,284*.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/01, 04/07/03*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

U.S. Patent and Trademark Office

PTOL-326 (Rev. 1-04)   Office Action Summary   Part of Paper No./Mail Date 09102004

DETAILED ACTION

1.   This action is in response to the preliminary amendment filed on 10/19/2001.

2.   Claims 29-32 and 45-48 are pending.

Priority

3.   An application in which the benefits of an earlier application are desired must contain a

specific reference to the prior application(s) in the first sentence of the specification of in

an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any

prior nonprovisional application must include the relationship (i.e., continuation,

divisional, or continuation-in-part) between the applications except when the reference is

to a prior application of a CPA assigned the same application number.

4.   Acknowledgment is made of applicant's claim for foreign priority under 35

U.S.C. 119(a)-(d). The certified copies have been received on 06/03/1999.

Information Disclosure Statement

5.   An initialed and dated copy of Applicant's IDS form 1449 received on 04/07/2003 and

10/19/2001 is attached to the instant Office action.

The content of information disclosure statement received on 10/19/2001, the foreign patent

document the abstract is only considered because the abstract is provided in English. For the full

document consideration full English version is required.

Claim Rejections - 35 USC § 101

6.   35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and
useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7.   Claim 29 is rejected under 35 U.S.C. 101 because the claimed invention is directed to

non-statutory subject matter.

The claim is non-statutory because it recite components of generating instruction

sequence from source code, representing functional descriptive material without a computer

readable medium or computer implemented, program per se are not tangibly embodied. Claims

29-32 thus amounts to only abstract idea and are nonstatutory.

Claim Rejections - 35 USC § 102

8.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9.   Claims 29-32 and 45-48 are rejected under 35 U.S.C. 102(b) as being anticipated by US

Patent No. 5,559,975 to Christie et al. (hereinafter called Christie).

Per claim 29:

Christie disclose:

- A compiler that generates an instruction sequence from source code (col. 5, lines 11-12 "Instructions decoder 108 examines the instructions and determined the appropriate action"),

- the compiler generating a program counter relative value calculating instruction that is executed by a processor (col. 5, lines 9-10 "a fetch program counter value which I generated by instructions cache"), the program counter relative value calculating instruction being an instruction that performs a calculation using a first value and a program counter relative value and uses a result of the calculation to update the first value, the first value being one of

- (a)a value of a program counter stored in a register (col. 6, lines 11-12 "program counter value is also stored in a program counter register in register file 112"), and

- (b)the value stored in a program counter of the processor (Abstract, "A processor which includes a fetch program counter circuit and an execute program counter"),

- wherein upper bits of the first value indicate a memory address at which a processing packet is stored (col. 9, lines 46-49 "Byte queue... upon detecting... indicates the byte of the target and the new target address to decode program counter" and (col. 11, lines 3-5 "Incrementer 330 receives the upper 28 bits... provides an incremented decode PC value"), and lower bits of the first value of the program counter indicate a processing target instruction that is included in the processing packet (col. 9, lines 51-52 "program counter value... provided to branch section 135 as well as low order bits and carry bits of the decode program counter value for each dispatched ROP").

Per claims 30 and 31:

Christie disclose:

- wherein the processor includes a lower bit calculating unit and an upper bit calculating

  unit (col. 10, lines 11-15 "program counter generator circuit 242 includes... less

  significant portion program counter latch 306, more significant portion program counter

  generator circuit 308"),

- the program counter relative value calculating instruction having the lower bit calculating

  unit perform a lower bit calculation (col. 10, lines 60-61 "Less significant program

  counter generator circuit 310 provides the carry bits from each adder to carry selector

  334") and the upper bit calculating unit perform an upper bit calculation (col. 10 and col.

  11, lines 66-67 and 1 "More significant program counter latch 304 provides bits 4:31 of

  the next program counter value to more significant program counter generator circuit

  308"),

- the lower bit calculation being an addition using lower bits of the first value and lower

  bits of the value of the program counter relative value (col. 11, lines 28-29 "allocate

  multiplexers 338 receive the lower order next program counter values (LPC)"), where a

  result of the lower bit calculation is set as the lower bits of the first value (col. 11, lines

  21-23 "Multiplexer... selects one of four potential lower order next program counter

  values as bits 0:3") and any generated carry is sent to the upper bit calculating unit (col.

  11, lines 30-31 "the carry values (CARRY) and provide these values to reorder buffer

  114 for each ROP that is dispatched"), and

-    the upper bit calculation being an addition using upper bits of the first value (col. 12,

     lines 3-5 "Incrementer 330 receives the upper 28 bits of the present decode PC value... a

     value in which the upper 28 bits are incremented by one"), upper bits of the value of the

     program counter relative value and any carry received from the lower bit calculating unit

     (col. 11, lines 11-12 "Carry selector circuit 334 uses the carry bits from less significant

     portion program counter"), where a result of the upper bit calculation is set as the upper

     bits of the first value (col. 11, lines 14-17 "If the carry bit of the next ROP to be

     dispatched is active... then the incremented decode PC value is used for the upper 28 bits

     of the next decode PC value").

Per claim 32:

Christie disclose:

-    wherein the processor includes an upper bit calculating unit (col. 10, lines 11-15

     "program counter generator circuit 242 includes...more significant portion program

     counter generator circuit 308"),

-    the program counter relative value calculating instruction having the upper bit calculating

     unit perform an upper bit calculation and setting lower bits of the program counter

     relative value as lower bits of the first value (col. 10 and col. 11, lines 66-67 and 1 "More

     significant program counter latch 304 provides bits 4:31 of the next program counter

     value to more significant program counter generator circuit 308"), and

-    the upper bit calculation being an addition using upper bits of the first value (col. 12,

     lines 3-5 "Incrementer 330 receives the upper 28 bits of the present decode PC value... a

value in which the upper 28 bits are incremented by one") and upper bits of the value of

the program counter relative value (col. 11, lines 11-12 "Carry selector circuit 334 uses

the carry bits from less significant portion program counter"), where a result of the upper

bit calculation is set as the upper bits of the first value (col. 11, lines 14-17 "If the carry

bit of the next ROP to be dispatched is active... then the incremented decode PC value is

used for the upper 28 bits of the next decode PC value").

Claims 45-48 are the computer program product claim corresponding to method claims 28-32

respectively, and rejected under the same rational set forth in connection with the rejection of

claims 28-32 respectively, above.

Substantially as claimed.

Conclusion

10.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to **Satish S. Rampuria** whose telephone number is **703-305-8891**.

The examiner can normally be reached on **8:30 am to 5:00 pm**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, **Kakali Chaki** can be reached on **(703) 305-9662**. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit 2124
09/20/2004

ANIL KHATRI
PRIMARY EXAMINER